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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/942,102	08/29/2001	William R. Wheeler	10559-595001 / P12879	6907

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EXAMINER	
THOMPSON, ANNETTE M	
ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 07/30/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/942,102	Applicant(s) WHEELER ET AL.	
	Examiner A. M. Thompson	Art Unit 2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 May 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8,10-18,20-28 and 30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8,10-18,20-28 and 30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 August 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Applicants' Reply in application 09/942,102 has been examined. The specification is amended. Claims 9, 19, and 29 are cancelled. Claims 1, 8, 11, 21, and 28 are amended. Claims 1-8, 10-18, 20-28 and 30 are pending.

1. Applicants' amendment obviates the existing objections. However, pursuant to further examination, the claims of the instant application remain rejected.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Rejection of claims 1-8, 10-18, 20-28 and 30

3. Claims 1-8, 10-18, 20-28 and 30 are rejected under 35 U.S.C. 102(b) as being anticipated by Rostoker et al. (Rostoker), U.S. Patent 5,544,067. Rostoker teaches a system for interactive design, synthesis and simulation of an electronic system allowing a user to design a system by specification of a behavioral model in a high level language such as VHDL or by graphical entry.

4. Pursuant to claim 1, which recites [a] method of generating a logic design (col. 12, ll. 40-4) for use in designing an integrated circuit comprising embedding a combinatorial one-dimensional logic block representing a combinatorial element within a two-dimensional schematic representation of the logic design to produce a unified database representation of the logic design (col. 25, line 60 to col. 26, line 64); wherein

the two-dimensional schematic representation includes a set of Register Transfer Diagrams (col. 6, ll. 47-61; col. 10, ll. 2-13; col. 10, ll. 47-64; see also Figure 18, which contains state data; col. 28, ll. 50-55).

5. Pursuant to claim 2, further comprising generating the combinatorial one-dimensional logic block (col. 27, ll. 19-40).

6. Pursuant to claim 3, further comprising importing the combinatorial one-dimensional logic block (col. 27, ll. 34-42).

7. Pursuant to claim 4, further comprising following a set of design capture rules (col. 27, line 59 to col. 28, line 17).

8. Pursuant to claim 5, further comprising notifying a designer when capturing data violates the set of design capture rules (col. 1, ll. 44-63, col. 9, ll. 16-36).

9. Pursuant to claim 6, further comprising using a set of abstractions (col. 7, ll. 4-13).

10. Pursuant to claim 7, further comprising generating C++ from the unified database (col. 2, ll. 51-65 and col. 23, ll. 11-34, wherein Prolog is the computer language).

11. Pursuant to claim 8, further comprising generating Verilog from the unified database (col. 13, line 40 to col. 14, line 17).

12. Pursuant to claim 10, further comprising generating synthesizable Verilog from the unified database (col. 13, line 40 to col. 14, line 17).

13. Pursuant to claim 11, which recites [a]n article comprising a machine-readable medium which stores executable instructions to generate a logic design for use in designing an integrated circuit (IC) (Fig. 16 illustrates these limitations); the instructions

causing a machine to: embed a combinatorial one-dimensional logic block representing a combinatorial element within a two-dimensional schematic representation of the logic design to produce a unified database representation of the logic design (col. 25, line 60 to col. 26, line 64); wherein the two-dimensional schematic representation includes a set of Register Transfer Diagrams (col. 6, ll. 47-61; col. 10, ll. 2-13; col. 10, ll. 47-64; see also Fig. 18, which contains state data; col. 28, ll. 50-55).

14. Pursuant to claims 12 and 22, these claims address limitations already rejected in claim 2, supra, and are likewise rejected here based on similar reasoning.

15. Pursuant to claims 13 and 23, these claims address limitations already rejected in claim 4, supra, and are likewise rejected here based on similar reasoning.

16. Pursuant to claims 14 and 24, these claims address limitations already rejected in claim 3, supra, and are likewise rejected here based on similar reasoning.

17. Pursuant to claim 21 which recites [a]n apparatus for generating a logic design for use in designing an integrated circuit, comprising a memory that stores executable instructions; and a processor that executes the instructions to (Fig. 16 illustrates these limitations): embed a combinatorial one-dimensional logic block representing a combinatorial element within a two-dimensional schematic representation of the logic design to produce a unified database representation of the logic design (col. 25, line 60 to col. 26, line 64); wherein the two-dimensional schematic representation includes a set of Register Transfer Diagrams (col. 6, ll. 47-61; col. 10, ll. 2-13; col. 10, ll. 47-64; see also Fig. 18, which contains state data; col. 28, ll. 50-55).

18. Pursuant to claims 15-18 and 20 and 25-28 and 30, these claims address limitations already rejected in claims 5-8 and 10, respectively, and therefore claims 15-18 and 20 and 25-28 and 30 are likewise respectively rejected here based on similar reasoning.

Rejection of claims 1-8, 10-18, 20-28 and 30

19. Claims 1-8, 10-18, 20-28 and 30 are rejected under 35 U.S.C. 102(b) based upon a public use or sale of the invention. Based on the Renoir datasheets, the Mentor Graphics Renoir tool that uses HDL2Graphics, discloses the limitations of Applicants' claimed invention in entirety.

20. The Renoir datasheets discloses a method of generating a logic design wherein combinatorial one-dimensional logic block is embedded with a two dimensional schematic representation of the design to produce a unified database representation; wherein the two-dimensional schematic representation includes a set of Register Transfer Diagrams.

21. An issue of public use or on sale activity has been raised in this application. In order for the examiner to properly consider patentability of the claimed invention under 35 U.S.C. 102(b), additional information regarding this issue is required as follows: Please submit a copy of the User's Manual for this product.

Applicant is reminded that failure to fully reply to this requirement for information will result in a holding of abandonment.

Claim Rejections - 35 USC § 103

22. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

23. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Rejection of claims 7, 8, 17, 18, 27 and 28

24. Claims 7, 8, 17, 18, 27, and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rostoker. Rostoker teaches a system for interactive design, synthesis and simulation of an electronic system allowing a user to design a system by specification of a behavioral model in a high level language such as VHDL or by graphical entry. Rostoker does not explicitly teach the use of C++ or Verilog. However, Applicant's specification at page 9, lines 8-18 clarifies that in this case, C++ is merely representative of any computer language. Rostoker discloses the use of Prolog (also a computer language like C++) which may be generated from its database, and to one of

ordinary skill in the art at the time of Applicants' invention, this disclosure would be sufficient to at least suggest Applicants' claims. Further, Rostoker discloses VHDL and Applicants' specification (page 9, lines 8-18) does not distinguish between the use of VHDL and Verilog. Therefore it would have been obvious to one of ordinary skill in the art that in this case, Rostoker's use of VHDL is at least within the scope of Applicants' claimed use of Verilog.

Remarks

25. Upon reconsideration, all pending claims now stand rejected. Claims 9, 19 and 29 recite Register Transfer Diagrams. However, Applicants' specification at page 3 defines the limitation of Register Transfer Diagrams as two-dimensional representations that convey or illustrate state elements of an IC design. Rostoker discloses this feature and the pertinent cites are referenced herein, supra. Therefore, these claims are not considered allowable over Rostoker. Further claims 7, 17, and 27 recite the limitation of generating C++ from the unified database. However, Applicant's specification at page 9, lines 8-18 clarifies that in this case, C++ is merely representative of any computer language. That being the case, Rostoker discloses the use of Prolog which may be generated from its database, and this disclosure is sufficient to at least suggest Applicants' claims. This same argument applies to claims 8, 18 and 28 which recites generating Verilog. Rostoker discloses VHDL and Applicants' specification (page 9, lines 8-18) does not distinguish between the use of VHDL and Verilog.

Conclusion

26. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to A.M. Thompson whose telephone number is (703) 305-7441. The Examiner can usually be reached Monday thru Friday from 8:00 a.m. to 5:00 p.m.. If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Matthew S. Smith, can be reached on (703) 308-1323.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956 or the Customer Service Center whose telephone number is (703) 306-3329.

27. Responses to this action should be mailed to:

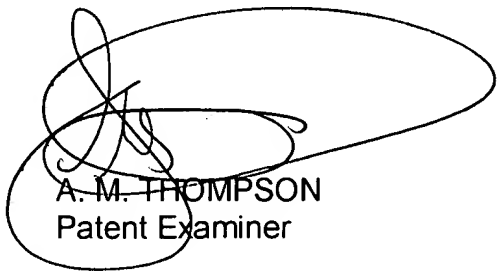
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

or faxed to:

(703) 872-9318, (for **OFFICIAL** communications intended for entry)

(703) 872-9319, (for Official **AFTER-FINAL** communications)

Hand-delivered responses should be brought to Crystal Plaza 4, 2021 South Clark Place, Arlington, VA., Fourth Floor (Receptionist).



A. M. THOMPSON
Patent Examiner